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PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the application of:

Attorney Docket No.: 3020.02US02

Meyer

Confirmation No.: 2544

Application No.: 09/899,763

Examiner: Not Assigned

Filed: July 5, 2001

Group Art Unit: 2123

For: DIGITAL AND ANALOG MIXED SIGNAL SIMULATION

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents  
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Sir:

Pursuant to 37 C.F.R. § 1.56, and in addition to information disclosed in Applicant's Information Disclosure Statement filed April 16, 2002, the attention of the Patent and Trademark Office is hereby directed to the references listed on the attached Form PTO-1449. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the references be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

This information is being filed before the mailing date of a first Office Action on the merits. No certification or fee is required.

I hereby certify that each item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(1). A copy of the Supplementary European Search Report is

enclosed for the Examiner's convenience. The two (2) U.S. references were cited in Applicant's previously filed Information Disclosure Statement.

Respectfully submitted,



Kimberly K. Baxter  
Registration No. 40,504

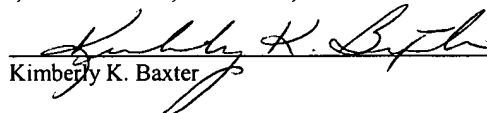
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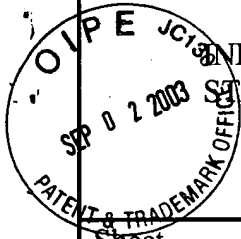
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INFORMATION DISCLOSURE  
STATEMENT BY APPLICANT  
(Use as many sheets as necessary)

Complete if Known

Application Number	09/899,763
Filing Date	July 5, 2001
First Named Inventor	Meyer
Art Unit	2123
Examiner Name	Not Assigned
Attorney Docket Number	3020.02US02

Sheet 1 of 1

## NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL*	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T <sup>2</sup>
		<i>Electronic Circuit Simulation in a Mixed-Language Environment</i> , Litovski et al., Microelectronics Journal, Mackintosh Publications Ltd., Vol. 29, No. 8, August 1, 1998; pgs. 553-558.	
		<i>Hardware Description Languages for ALECSIS Simulator</i> , Damnjanovic et al., Microelectronics 1995 Proceedings, New York, IEEE, September 1995, pgs. 525-528.	
		Verilog-AMS Language Reference Manual, Open Verilog International, December 1999, Los Gatos, California, Chapter 9.	
		<i>On the Design of Mixed-Mode Simulators for Modern VLSI Circuits</i> , Abdallah et al., Circuits and Systems Proceedings 1995, New York, IEEE, August 1995, pgs. 1168-1171.	
		<i>A System-Level Simulation Environment for System-on-Chip Design</i> , Schneider et al., 13 <sup>th</sup> Annual IEEE International ASIC/SOC Conference, September 2000, Washington, D.C., pgs. 58-62.	

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This collection of information is required by 37 CFR 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 120 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450.

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